Unit - 19 Semiconductor Electronics

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SUMMARY

- **Conductor :- •** Presence of free electrons
 - Electrical resistivity is quite less
- Insulator :- No free electrons
 - Very large electrical resistivity

Semi-conductor :-

- Electrical resistance greater than conductor but smallar than insulator
- At O K temperature it behaves like perfect insulator (in pure form)
- Hole: An empty space, when covalent bond breaks and electron gets escaped.
 - It is electron deficiency space called hole
 - behaves like positive electric charge.

For intrinsic (pure) semi-conductor :-

- $n_i = n_e = n_h$ where $n_i =$ Intrinsic electrical charge carrier density, $n_e =$ number density of electrons $n_h =$ number density of holes
- Electrical conduction is due to both, electrons and holes

* Extrinsic semi-conductor :-

- (1) N-type : Pentavalent impurity is added
 - Majority charge carrier are electrons
 - $n_e > n_h$
- (2) P-type : Trivalent imparity is added
 - Majority charge carries are holes
 - $n_h > n_e$
- * Valence Band :- Completely filled (with 4N electrons) lower band is called valence band
- * Forbidden Gap :- The region above valance band without any available energy levels is called forbidden gap
- * Conduction Band :- The region above forbidden gap is called conduction band
- * Band Gap (Eg) :- The difference between minimum energy (Ec) of conduction band and maximum energy (Ev) of valence band is known as band gap energy
 - For Insulator Eg > 3eV
 - For Conductor Eg = 0
 - For semiconductor Eg < 3eV



- * Depletion Region :-
 - A region near the junction which is deplete of respective majority charge carriers.
 - Thickness is about $0.5 \,\mu$ m
- * **Depletion Barrier :-** The varying electrical potential near junction is called depletion barrier (0.7V for Si and 0.3V for Ge)
- * Forward Bias :-
 - When P end of PN junction is connected to positive pole of the battery and N end is connected to negative pole of the battery, then such an arrangement is called forward bias.
 - Depletion barrier (P.d) and Depletion region (width) is decreased.
- * Reverse Bias :-
 - When P end of PN junction is connected to negative pole of the battery and N end is connected to positive pole of the battery, then such an arrangement is called forward bias.
 - Depletion barrier (P.d) and depletion region (width) are increased
- * Brekdown voltage :- In reverse bias condition of PN junction, for certain voltage, current increases suddenly. This certain voltage is called breakdown voltage.
- * Zener effect :- Due to smaller width of depletion region even at small reverse bias voltage, electric field becomes strong enough to break covalent bond, giving large number of electron hole pair is called zener effect
- * Avalanche effect :- Due to large width of depletion region, at only high reverse bias voltage electric field in the depletion region becomes strong enough to break many covalent bonds, giving rise to so many charge carrier is called avalanch effect and diode is called avalanche diode
- * **Regulated Power Supply :-** If D.C. output voltage, in a rectifier circuit (or power supply) remains constant with the charge in load current I, then such power supply is called reguluted power supply
- * Rectification and Rectifier :- The process of obtaining D.C. voltage (or current) from A.C. voltage (or current) is called rectification and circuit assembled for this process is called rectifier
- * TRANSISTOR
 - Transistor is a device made of two PN junctions
 - Junction between base and emitter is called emitter junction
 - Junction between base and collector is called collector junction
 - For proper working of transistor, emitter junction should be forward biased and collector junction should be reverse biased
 - A.C. parameters for a transistor

(1) Input resistance =
$$r_i = \left[\frac{\Delta V_{BE}}{\Delta I_B}\right]_{V_{CE}=constant}$$

(2) Output resistance =
$$r_0 = \left[\frac{\Delta V_{CE}}{\Delta I_C}\right]_{I_B = constant}$$

(3) A.C. current gain =
$$A_i = \beta_{ac} = \left[\frac{\Delta Ic}{\Delta I_B}\right]_{V_{CE} = constant}$$

(4) Transconductance =
$$g_m = \frac{\Delta I_C}{\Delta V_{BE}} = \frac{\beta ac}{r_i}$$

- D.C. Parameters of a transistor
 - (1) $I_{E} = I_{B} + I_{C}$
 - (2) Current gain for CB circuit $=\alpha_{dc} = \frac{I_C}{I_E}$
 - $\alpha_{dc} < 1$
 - (3) Current gain for CE cicuit = $\beta_{dc} = \frac{I_C}{I_B}$
 - $\beta_{dc} >> 1$
- Voltage gain for CE Amplifier

$$Av = \frac{\Delta V_{CE}}{\Delta V_{BE}} = -\frac{\beta_{ac}}{r_i} R_L = -g_m R_L$$

• Power gain for CE Amplifier

$$\mathbf{A}_{\mathrm{p}} = \mathbf{A}_{\mathrm{v}} \times \mathbf{A}_{\mathrm{i}} = \beta_{\mathrm{ac}}^{2} \frac{\mathbf{R}_{\mathrm{L}}}{\mathbf{r}_{\mathrm{i}}}$$

* Oscillator :- Certain electronic circuits can generated any arbitrary frequency with desired amplitude of voltage and current. Such circuit is known as oscillator.

• Oscillator frequency
$$= f = \frac{1}{2\pi\sqrt{LC}}$$

- * Logic gate :-
 - The logic circuit, with one or more than one input but only one output is called logic gate.
 - Basic logic gates are OR gate, AND gate and NOT gate
 - Universal logic gates are NAND gate and NOR gate

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* LOGIC GATES

- A digital circuit with one or more input signals but only one output signal is known as logical gate.
- □ The logic gates are the building blocks of a digital system. Each logic gate follows a certain logical relationship between input and output voltage.
- □ There are three basic logic gates :
 - O OR gate
 - AND gate
 - O NOT gate

Truth table

□ It is a table that shows all possible input combinations and corresponding output combination for a logic gate.

OR gate

- □ An OR gate has two or more inputs but only one output.
- It is called OR gate because the output is high if any or all the inputs are high.
- □ The logic symbol of OR gate is



• The truth table for OR gate is

Inpu	ıt	Output	
А	В	Y	
0	0	0	
0	1	1	
1	0	1	
1	1	1	

D The Boolean expression for OR gate is

$$\mathbf{Y} = \mathbf{A} + \mathbf{B}$$

AND gate

- An AND gate has two or more inputs but only one output.
- It is called AND gate because output is high only when all the inputs are high.
- □ The logic symbol of AND gate is



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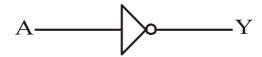
• The truth table for AND gate is

Input		Output
A B		Y
0	0	0
0 1		0
1	0	0
1	1	1

 $\Box \qquad \text{The Boolean expression for AND gate is } Y = A \cdot B$

NOT gate

- The NOT gate is the simplest of all logic gates. It has only one input and one output.
- □ NOT gate is also called inverter because it inverts the input.
- □ The logic symbol of NOT gate is



• The truth table for NOT gate is

Input	Output	
А	Y	
0	1	
1	0	

 $\Box \quad \text{The Boolean expression for NOT gate is } Y = \overline{A}$

NAND gate

- □ It is an AND gate followed by a NOT gate.
- □ The logic symbol for NAND gate is



• The truth table for NAND gate is

Inpu	t	Output
А	В	Y
0	0	1
0	1	1
1	0	1
1	1	0

□ The Boolean expression for NAND gate is

 $Y = \overline{A \cdot B}$

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NOR gate

- □ It is an OR gate followed by a NOT gate.
- The logic symbol of NOR gate is



□ The truth table for NOR gate is

Input		Output	
А	В	Y	
0	0	1	
0	1	0	
1	0	0	
1	1	0	

□ The Boolean expression for NOR gate is

 $Y = \overline{A + B}$

Exclusive OR gate or XOR gate

□ The logic symbol of XOR gate is



• The truth table for XOR gate is

Input		Output	
А	В	Y	
0	0	0	
0	1	1	
1	0	1	
1	1	0	

• The Boolean expression for XOR gate is

$$Y = \overline{A} \cdot B + A \cdot \overline{B} = A \oplus B$$

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Exlusive NOR gate or XNOR gate

□ The logic symbol of XNOR gate is



□ The truth table for XNOR gate is

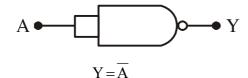
Input		Output	
А	В	Y	
0	0	1	
0	1	0	
1	0	0	
1	1	1	

□ The Boolean expression for XNOR gate is

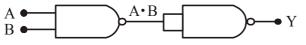
 $Y \!=\! A \!\cdot\! B \!+\! \overline{A} \!\cdot\! \overline{B} \!=\! \overline{A \!\oplus\! B}$

NAND as a universal gate

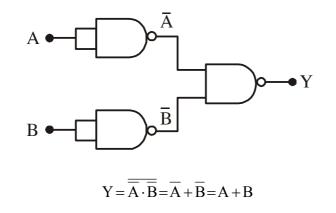
- NAND gate is called as universal gate because with the repeated use of NAND gate we can construct any basic gate
- □ NOT gate from NAND gate



□ AND gate from NAND gates



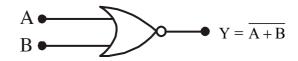
□ OR gate from NAND gates



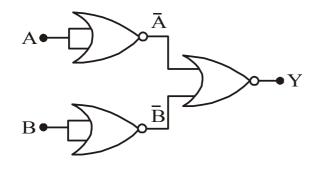
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NOR gate as a universal gate

- □ NOR gate is called as universal gate because with the repeated use of NOR gate we can construct any basic gate.
- □ NOT gate from NOR gate

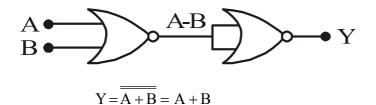


□ AND gate from NOR gate



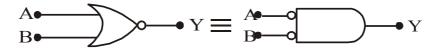
$$Y = \overline{\overline{A} + \overline{B}} = \overline{\overline{A} \cdot \overline{B}} = A \cdot B$$

□ OR gate from NOR gate



De Morgan's Theorems

 $\Box \qquad \overline{A+B} = \overline{A} \cdot \overline{B}$



NOR gate is equivelent to bubbled AND gate.

 $\Box \qquad \overline{\mathbf{A} \cdot \mathbf{B}} = \overline{\mathbf{A}} + \overline{\mathbf{B}}$



□ NAND is equivalent to bubbled OR gate.

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Boolean identities

A + B = B + A	$\mathbf{A} \cdot \mathbf{B} = \mathbf{B} \cdot \mathbf{A}$
A + (B + C) = (A + B) + C	$\mathbf{A} \cdot (\mathbf{B} \cdot \mathbf{C}) = (\mathbf{A} \cdot \mathbf{B}) \cdot \mathbf{C}$
$\mathbf{A} \cdot (\mathbf{B} + \mathbf{C}) = \mathbf{A} \cdot \mathbf{B} + \mathbf{A} \cdot \mathbf{C}$	$\mathbf{A} + \mathbf{B} \cdot \mathbf{C} = (\mathbf{A} + \mathbf{B}) \cdot (\mathbf{A} + \mathbf{C})$
A + 0 = A	$A \cdot 1 = A$
A + 1 = 1	$\mathbf{A} \cdot 0 = 0$
A + A = A	$A \cdot A = A$
$A + \overline{A} = 1$	$A \cdot \overline{A} = 0$
$\overline{\overline{A}} = A$	$\overline{\overline{A}} = A$
$\overline{A+B} = \overline{A}.\overline{B}$	$\overline{A.B} = \overline{A} + \overline{B}$
$\mathbf{A} + \mathbf{A} \cdot \mathbf{B} = \mathbf{A}$	$\mathbf{A} \cdot (\mathbf{A} + \mathbf{B}) = \mathbf{A}$
$A + \overline{A} \cdot B = A + B$	$A \cdot \left(\overline{A} + B\right) = A \cdot B$

<u>MCQ</u>

For the answer of the following questions choose the correct alternative from among the given ones.

C, Si and Ge have same no. of valence electrons. C is an insulator because energy required to take one (1)electron out from (A) Si is more (B) C is more (C) Ge is more (D) C is less (2)Ionization energy of isolated phosphorous atomis 10 eV. Ionization energy of same atom in Si is nearly _____ eV (Relative Permitivity of silicon = 12) (A) **0.1** (B) **0.2** (C) 0.3 (D) 0.4 (3) By adding ______ impurity in intrinsic semiconductor P type semiconductor is made. charge of these P type semiconductor is _____ (A) trivalent, neutral (B) pentaralent, neutral (C) pentavalent, positive (D) trivalent, negative (4)Strong overlaping of different atomic orbitals makes (A) different energy level (B) energy band (C) Conductor (D) Insulators (5) We can not make p-n junction diode by making P type semi-condutor join with N - type semi-conductor, because (A) Inter-atomic spacing becomes less than 1A^o (B) P - type will repel N - type (C) There will be discontinuity for the flowing charge carriers (D) semi-conducting properties will be lost 330

- (6) For p-n junction, which statement is incorrect
 - (A) Donor atoms are depleted of their holes in junction
 - (B) No net charge exists far from junction
 - (C) Barrier potential V_{B} is generated
 - (D) Energy $V_{\rm B}$ is to be surmounted before any charge can flow across junction
- (7) The intrinsic semi-conductor has :
 - (A) a finite resistance which does not change with temperature
 - (B) infinite resistance which decreases with temperature
 - (C) Finite resistance which decreases with temperature
 - (D) Finite resistance which does not change with temperature
- (8) The behaviour of Ge as semi-conductor is due to width of :
 - (A) Conduction band being large
 - (B) Forbidden band being large
 - (C) Conduction band being small
 - (D) Forbidden band being small and narrow
- (9) Which of the following is not the advantage of PN junction diode over tube valve ?
 - (A) Unlimited life
 - (C) Large efficiency
- (10) The forward biased diode is
- (10) The forward blased above is (A) $\stackrel{\circ}{\operatorname{ov}} \xrightarrow{} \stackrel{\circ}{\operatorname{ov}} \stackrel{\circ}{\operatorname{ov}} \stackrel{\circ}{\operatorname{ov}} \stackrel{\circ}{\operatorname{ov}} (B)$ (C) $\stackrel{\circ}{\operatorname{+sv}} \xrightarrow{} \stackrel{\circ}{\operatorname{ov}} \stackrel{\circ}{\operatorname{ov}} (D)$ (11) A g ble :

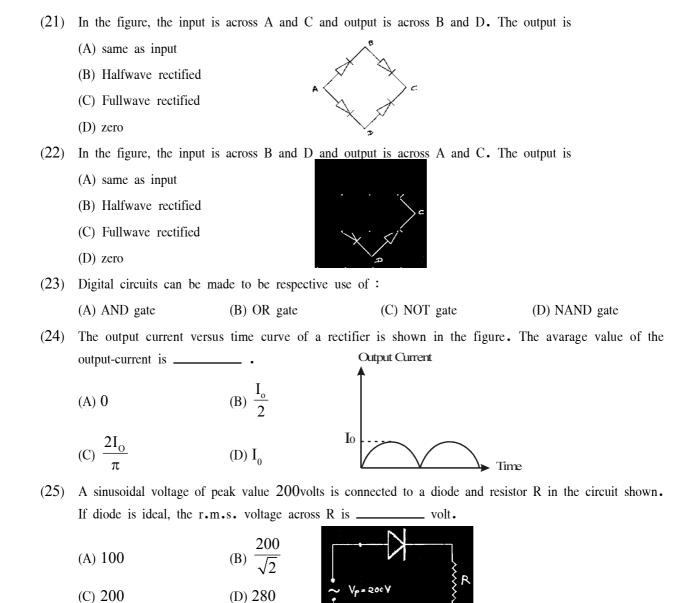
0	-4∨	-4∨		о ЗҮ
o −4V	-4V	-4V	-4V	• •
+1V		·······	V V -	-1V

ρ	a	R
0	0	1
0	1	1
1	0	1
1	1	0

The gate is :				
(A) OR	(B) NOR	(C) NAND	(D) AND	
		331		

- (B) No warming-up time after switching
- (D) Low consumption of Power

(12) A current gain for a transistor working as CB amplifier is 0.90. If emitter current is 10 mA, then base current is ____ (B) 2mA (C) 0.1 mA(A) 1 mA (D) 0.2 mA(13) For a transistor $\frac{I_C}{I_E} = 0.96$, then CE current gain is : (A) 12 (C) 24 (B) 6 (D) 48 (14) The given truth table is for which logic gate ? 'n 1 0 (A) XOR (B) AND (C) NAND (D) NOR (15) For the given circuit of ideal P.N junction diode which is correct ? R (A) In F.B, the voltage across R is V (B) In R.B, the voltage across R is V (C) In F.B, the voltage across R is -V (D) In R.B the voltage across R is -V (16) At \circ K temp, a N - type semi-conductor : (A) does not have any charge carriers (B) has few holes but no free electrons (C) few holes and few electrons (D) has equal number of holes and electrons (17) In Si-crystal, impurity donor atom have valency. (A) 2 (C) 4 (D) 5 (B) 3 (18) A N-P-N transistor conducts when collector is _____ and emitter is _____ with respect to base. (A) positive, negative (B) positive, positive (C) negative, negative (D) negative, positive (19) A full wave rectifier is operating at 50Hz, 220V the fundamental frequency of ripple will be _____. (A) 50 Hz (B) 75 Hz (C) 110 Hz (D) 100 Hz (20) Reverse bias applied on a junction diode : (A) raises the potential barrier (B) increases majority charge carrier current (C) lowers the potential barrier (D) increases the temperature of junction 332



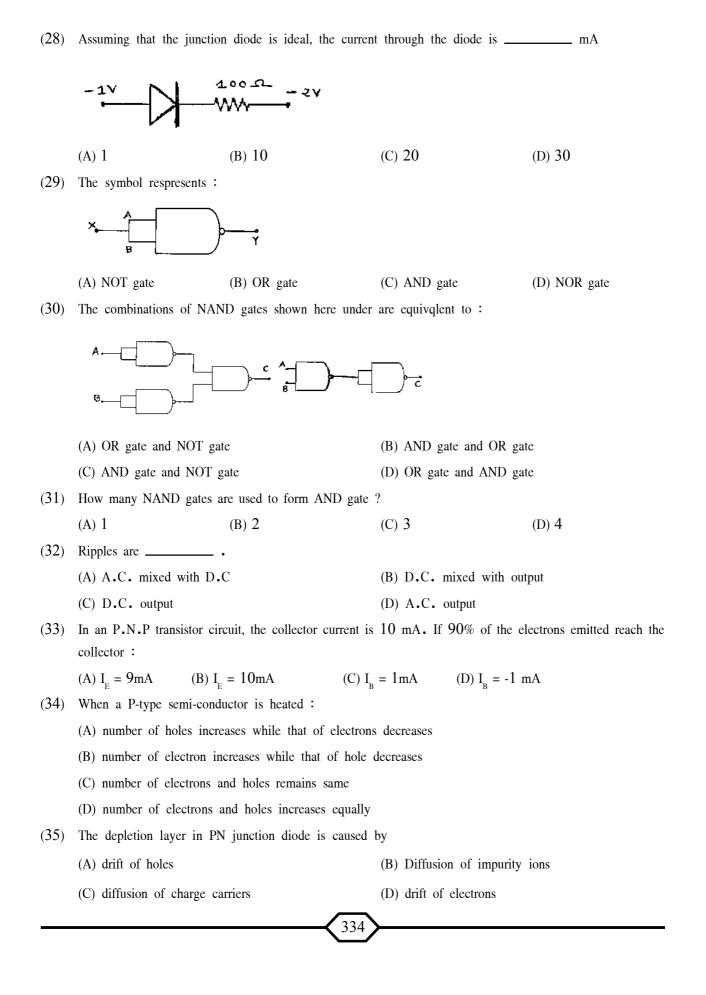
(26) For a transistor, in a common base configuration the alternating current gain α is given by :

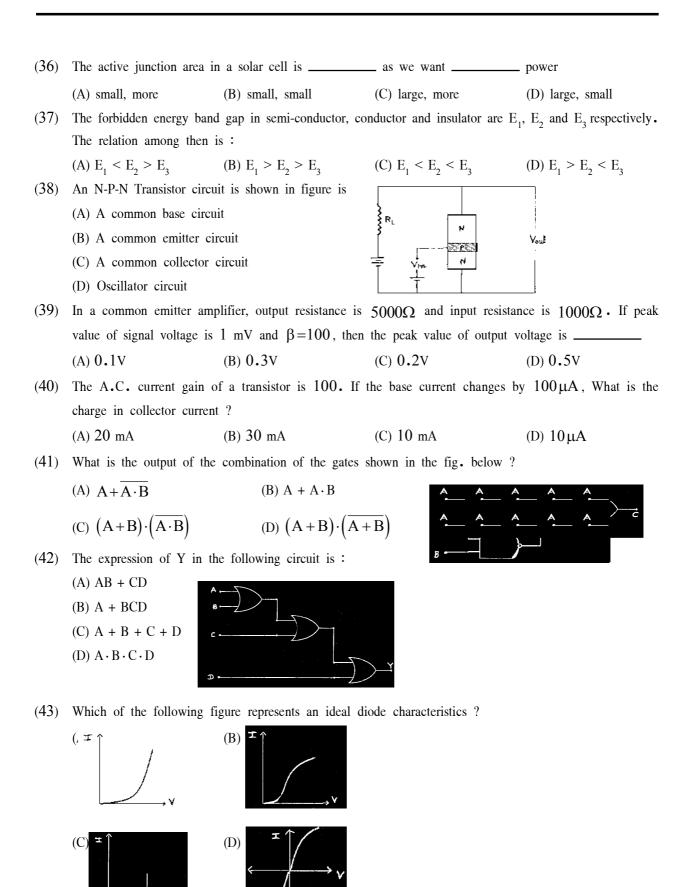
(A)
$$\left[\frac{\Delta I_{C}}{\Delta I_{B}}\right]_{V_{C}=\text{const.}}$$
 (B) $\left[\frac{\Delta I_{B}}{\Delta I_{C}}\right]_{V_{C}=\text{const.}}$
(C) $\left[\frac{\Delta I_{C}}{\Delta I_{E}}\right]_{V_{C}=\text{const.}}$ (D) $\left[\frac{\Delta I_{E}}{\Delta I_{C}}\right]_{V_{C}=\text{const.}}$

(27) In a N-P-N transistor circuit, the emitter, collector and base current are respectively I_{E} , I_{C} and I_{B} . The relation between them is ______.

(A)
$$I_{c} < I_{E} < I_{B}$$
 (B) $I_{B} < I_{c} < I_{E}$ (C) $I_{B} > I_{c} < I_{E}$ (D) $I_{B} > I_{c} > I_{E}$

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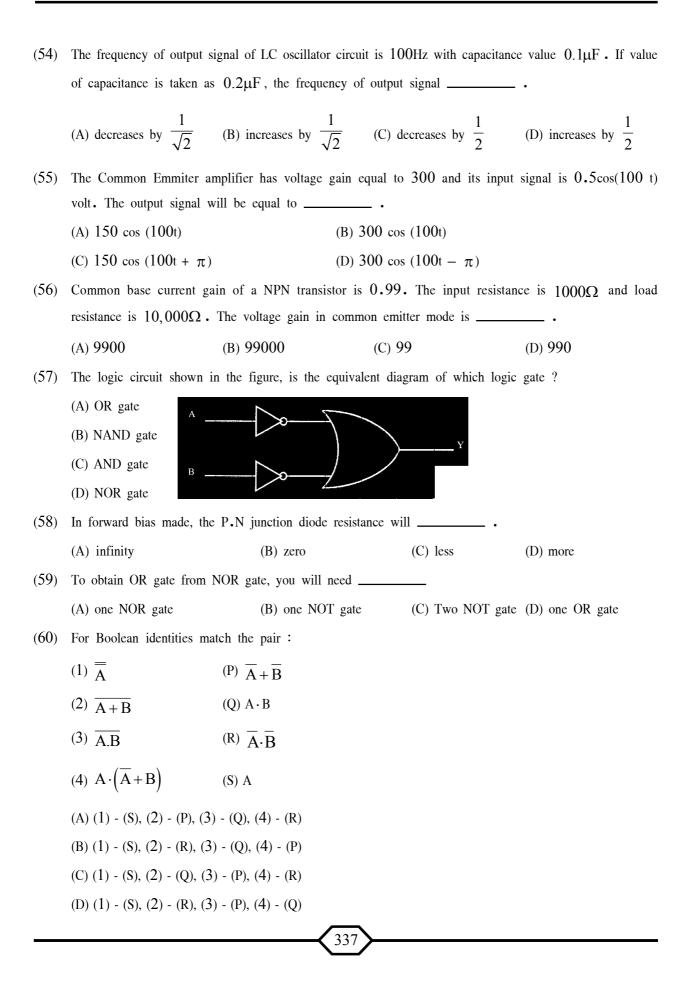


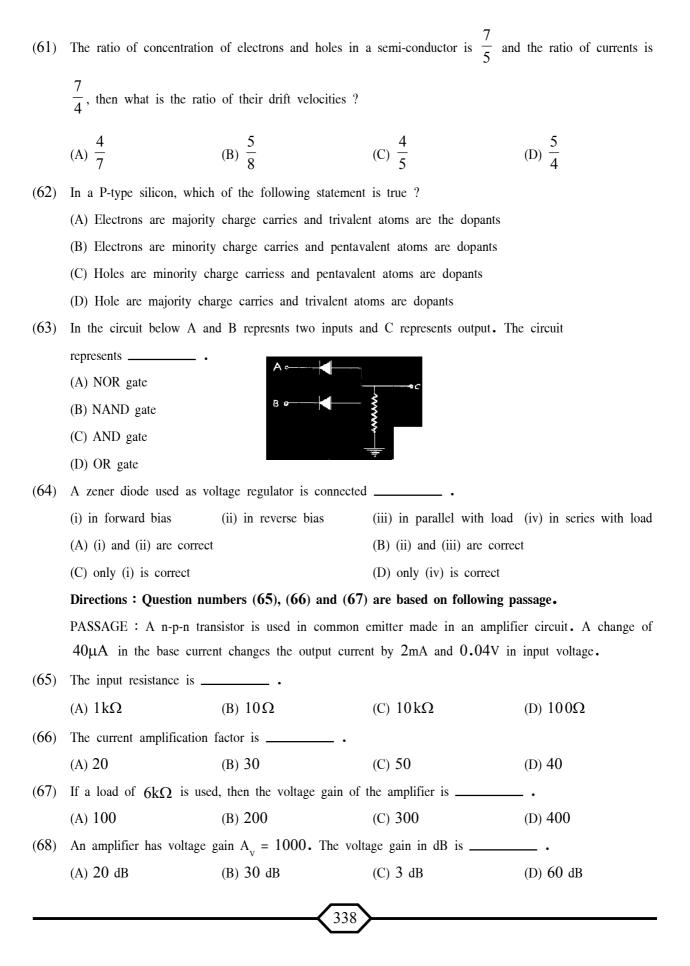


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(44)	In Ge sample, traces of gal	lium are added as impurit	v. The resultant sample w	ould behave like :	
()	(A) a conductor		(B) a P-type semiconducto		
	(C) an N-type semiconducto	o r	(D) an insulator		
(45)	•••			is passed. If this LED is	
()) A light emitting diode has a voltage drop of 2V across it when 10mA current is passed. If this is to be operated with 6V battery the value of limiting resistor would be				
	(A) 400Ω	(B) 4000Ω	(C) 40kΩ	(D) 300Ω	
(46)	NAND gate is				
	(A) A basic gate		(B) Not a universal gate		
	(C) A universal gate		(D) Multipurpose gate		
(47)	The number of holes and temperature. Which of the		-	respectively at room	
	(A) $x > y$	(B) $y > x$	(C) $\mathbf{x} = \mathbf{y}$	(D) x << y	
(48)	How will you increase the	resistivity of Ge semi-con	ductor ?		
	(A) On adding donor imput	rity	(B) On adding acceptor in	mpurity	
	(C) On making UV light in	cident on Ge crystal	D) On decreasing the temperature		
(49)	What is type of material, for	or the energy band diagrar	n shown in the figure ?		
	(B) P - type semi-conductor	r ^E c <u>///////</u>			
	(C) Insulator	$E_g = 1 e$	v		
	(D) Intrinsic semi-conductor		0.05 eV		
(50)	From the following semi-co	nductor devices,	operates in forward bi	as only.	
	(A) Varactar diode	(B) Zener diode	(C) Light emitting diode	(D) photo-diode	
(51)	device is the	odd-one out.			
	(A) solar-cell	(B) Varactor diode	(C) Photodiode	(D) Zener diode	
(52)	The value of depletion capa	acitance on o	decreasing the reverse bias	on varactor diode	
	(A) decreases	(B) increases	(C) becomes zero	(D) does not change	
(53)	Which of the following stat	tement is correct for trans	istor LC oscillator circuit ?	,	
	(A) It works with negative	feed back			
	 (B) The phase difference between output and input signal is π radian (C) To start oscillation external signal is required (D) The frequency of output signal is independent of the components used in feed back circuit 				

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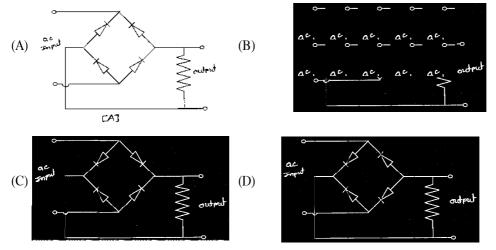




(69) A potential barrier of 0.6V exists across a P-N junction. If the depletion region is $1\mu m$ wide, what is the intensity of electric field in the region ?

(A)
$$4 \times 10^5 \text{Vm}^{-1}$$
 (B) $5 \times 10^5 \text{Vm}^{-1}$ (C) $6 \times 10^5 \text{Vm}^{-1}$ (D) $2 \times 10^5 \text{Vm}^{-1}$

- (70) when a PN junction diode is forward biased, then the depletion region is _____ and barrier height is _____ .
 - (B) widened, reduced (A) reduced, increases (C) reduced, reduced (D) increased, increased
- Which of the following circuit provides full wave rectification ? (71)



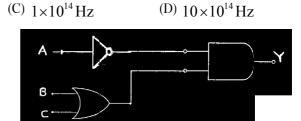
(72) A common- emitter amplifier has a voltage gain of 100, an input impedence of 100Ω and an output impedence of 200Ω . The product of voltage gain and current gain is _____ (B) 3000 (C) 5000 (A) 1000 (D) 500

- (73) A P-N photodiode is made of a material with a band gap of 2.0ev. The minimum frequency of the radiation that can be absorbed by the material is nearly (Take hc = 1240 eVnm)
 - (A) 5×10^{14} Hz (B) 20×10^{14} Hz
- (74) The bodean equation for the circuit is
 - (A) $Y = \overline{A} \cdot B + C$ (B) $Y = \overline{A} \cdot (B + C)$ (C) $Y = \overline{A} \cdot \left(\overline{B} + \overline{C}\right)$ (D) $Y = \overline{A} \cdot \left(B + \overline{C}\right)$

(75) A n-p-n transistor circuit has $\alpha = 0.985$. If I_c = 9 mA then the value of I_B is _____. (A) 0.003mA (B) **0.66**mA (C) **0.015**mA (D) 0.03mA

- (76) For a transistor amplifier, the voltage gain
 - (A) remains constant for all frequencies
 - (B) is high at high and low frequencies and constant in the mid-frequency range
 - (C) is low at high and low frequencies and constant in the mid-frequency range
 - (D) None of the above

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(77) The current flowing through 10Ω resistor in the circuit shown in the figure is _____.

(A) 50mA	(B) 20mA	
(C) 40mA	(D) 80mA	1

(78) The input and outputs from different time intervals are given below for NAND gate

Time interval	Input A	Input B	Output Y		
t ₁ to t ₂	0	1	Р		
t ₂ to t ₃	0	0	Q		
t ₃ to t ₄	1	0	R		
t ₄ to t ₅	1	1	S		
The surface taken has D. O. D. and C. and surgesting has					

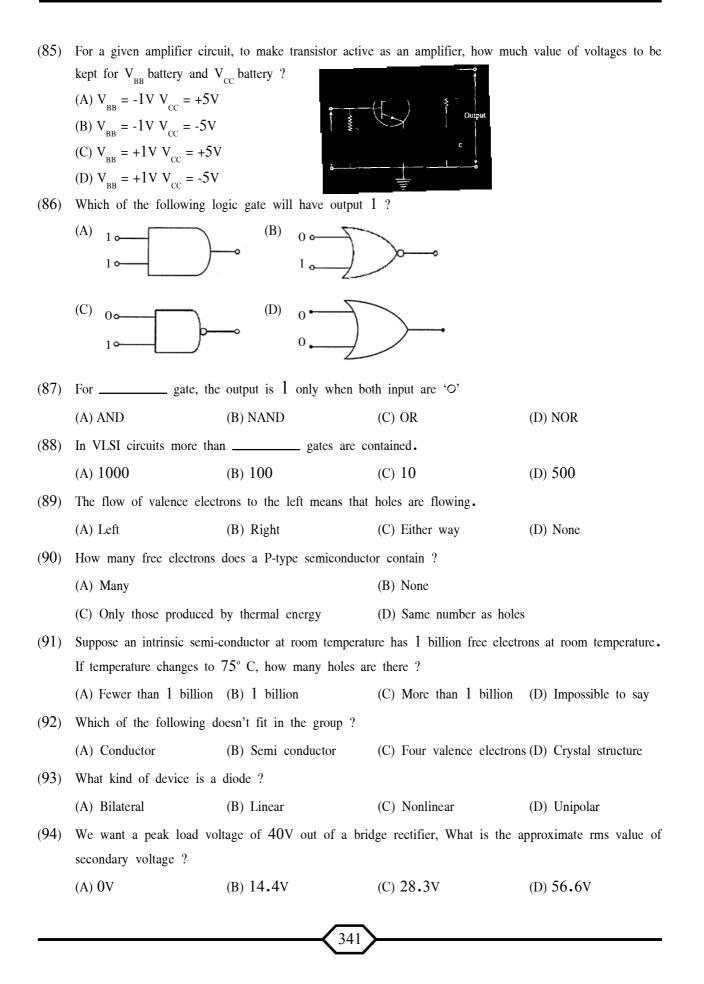
The value taken by P, Q, R and S are respectively

- (A) 1, 0, 1, 1 (B) 0, 1, 0, 0
- (79) The manifestation of band structure in solids is due to :
 - (A) Heisenberg's uncertainty principle
 - (B) Pauli's exclusion principle
 - (C) Bohr's correspondence principle
 - (D) Boltzmann's low
- (80) Copper and silicon material is cooled down from 600K to 400K then, resistivity of cooper ______ and silicon ______ .
- (A) increases, decreases
 (B) decreases, increases
 (C) decreases, decreases
 (D) increases, increases
 (81) Semi-conductor has phospholous as impurity then it will have ______.

(C) 0, 1, 0, 1 (D) 1, 1, 1, 0

- (A) $n_c \gg n_h$ (B) $n_c \ll n_h$ (C) $n_c = n_h$ (D) $n_c = n_h = n_i$
- (82) Zener diode is used as ______
 (A) Full. wave rectifier
 (B) amplifier
 (C) A.C. voltage regulator
 (D) D.C. voltage regulator
- (83) Break down voltage of a diode is 5V. By which effect this breakdown occurs in diode ?
 - (A) Only avalanche effect (B) Only zener effect
 - (C) Avalanche or zener effect (D) None of the above
- (84) When NPN transistor is used as an amplifier then _____
 - (A) electron moves from base to collector
 - (B) hole travels from emitter to base
 - (C) hole goes to emitter from base
 - (D) electron goes to base from collector

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(95)	The load-current is approximately constant when a	zener diode is	
()))	(A) Forward biased	(B) Reverse biased	•
	(C) Operating in breakdown region	(D) Unbiased	
(06)			anner in stale as start of
(96)	When source voltage increases in a zener diode, where the source voltage increases in a zener diode, where the source the source of the source		
(07)	(A) Series current (B) Zener current	(C) Load current	(D) Total current
(97)	The device associated with voltage controlled capa		
	(A) Light emitting diode (B) Photo diode	(C) Varactor diode	(D) Zener diode
(98)	For normal operation of the transistor, the collector (A)		·
	(A) Forward biased	(B) Reverse biased	
(00)	(C) Non conducting	(D) Operating in breakdo	own region
(99)	Most of the electrons in the base of N-P-N transist		
	(A) Out of the base lead (B) Into the collector	(C) Into the emitter	(D) Into the base supply
	Direction for Assertion - Reason type questions		
	(A) If both Assertion and Reason are true and r	eason is the correct explan	ation of assertion.
	(B) If both Assertion and Reason are true but R	eason is not the correct exp	planation of assertion.
	(C) If Assertion is true but Reason is false	eason is not the correct exj	planation of assertion.
	(C) If Assertion is true but Reason is false(D) If both assertion and reason are false		planation of assertion.
(100)	(C) If Assertion is true but Reason is false		planation of assertion.
(100)	(C) If Assertion is true but Reason is false(D) If both assertion and reason are false		planation of assertion.
(100)	(C) If Assertion is true but Reason is false(D) If both assertion and reason are falseA : Intrinsic charge carries are thermally generated		planation of assertion. (D)
	 (C) If Assertion is true but Reason is false (D) If both assertion and reason are false A : Intrinsic charge carries are thermally generated R : Their availability can be easily controlled 	(C)	
	 (C) If Assertion is true but Reason is false (D) If both assertion and reason are false A : Intrinsic charge carries are thermally generated R : Their availability can be easily controlled (A) (B) 	(C) rd or fourth group	
	 (C) If Assertion is true but Reason is false (D) If both assertion and reason are false A : Intrinsic charge carries are thermally generated R : Their availability can be easily controlled (A) (B) A : Impurity atoms for silicon is selected from thin 	(C) rd or fourth group	
(101)	 (C) If Assertion is true but Reason is false (D) If both assertion and reason are false A : Intrinsic charge carries are thermally generated R : Their availability can be easily controlled (A) (B) A : Impurity atoms for silicon is selected from thin R : These Impurity atoms have same size as that an another selection of the selectio	(C) rd or fourth group of Si	(D)
(101)	 (C) If Assertion is true but Reason is false (D) If both assertion and reason are false (A): Intrinsic charge carries are thermally generated (A): Their availability can be easily controlled (A) (B) (A): Impurity atoms for silicon is selected from thin (R): These Impurity atoms have same size as that of (A) (B) 	(C) rd or fourth group of Si (C)	(D)
(101)	 (C) If Assertion is true but Reason is false (D) If both assertion and reason are false (A): Intrinsic charge carries are thermally generated (R): Their availability can be easily controlled (A) (B) (A): Impurity atoms for silicon is selected from thin (R): These Impurity atoms have same size as that of (A) (B) (A): Photodiode are operated in reverse bias 	(C) rd or fourth group of Si (C)	(D)
(101)	 (C) If Assertion is true but Reason is false (D) If both assertion and reason are false (A): Intrinsic charge carries are thermally generated (A): Their availability can be easily controlled (A) (B) (A): Impurity atoms for silicon is selected from thin (R): These Impurity atoms have same size as that of (A) (B) (A): Photodiode are operated in reverse bias (R): In reverse bias fractional change in minority of 	(C) rd or fourth group of Si (C) charge carrier is more (C)	(D) (D)
(101)	 (C) If Assertion is true but Reason is false (D) If both assertion and reason are false (A): Intrinsic charge carries are thermally generated (A): Their availability can be easily controlled (A) (B) (A): Impurity atoms for silicon is selected from thin (R): These Impurity atoms have same size as that of (A) (B) (A): Photodiode are operated in reverse bias (A) (B) (A): Mathematical change in minority of (A) (B) 	 (C) rd or fourth group of Si (C) charge carrier is more (C) with temperature 	(D) (D)
(101)	 (C) If Assertion is true but Reason is false (D) If both assertion and reason are false (A) Intrinsic charge carries are thermally generated (A) Intrinsic charge carries are thermally generated from thing (A) Intrinsic charge in the second carries are the second charge in the second carries are the second ca	 (C) rd or fourth group of Si (C) charge carrier is more (C) with temperature 	(D) (D)
(101) (102) (103)	 (C) If Assertion is true but Reason is false (D) If both assertion and reason are false (A): Intrinsic charge carries are thermally generated (A): Their availability can be easily controlled (A) (B) (A): Impurity atoms for silicon is selected from thin (R): These Impurity atoms have same size as that of (A) (B) (A): Photodiode are operated in reverse bias (R): In reverse bias fractional change in minority of (A) (B) (A): The resistivity of a semi-conductor decreases of (R): At higher temperature more co-valent bond bit 	 (C) rd or fourth group of Si (C) charge carrier is more (C) with temperature reaks (C) 	(D) (D)
(101) (102) (103)	 (C) If Assertion is true but Reason is false (D) If both assertion and reason are false (A : Intrinsic charge carries are thermally generated (A : Their availability can be easily controlled (A) (B) (A : Impurity atoms for silicon is selected from thin (R : These Impurity atoms have same size as that of (A) (B) (A : Photodiode are operated in reverse bias (R : In reverse bias fractional change in minority of (A) (B) (A : The resistivity of a semi-conductor decreases of (A) (B) (A : At higher temperature more co-valent bond bit (A) (B) 	 (C) rd or fourth group of Si (C) charge carrier is more (C) with temperature reaks (C) ing blocks 	(D) (D) (D)

(105) A : The colour of light emitted by depends on its forward bias.					
R : The forward biasing of PN junction diode will increase the width of depletion layer					
(A)	(B)	(C)	(D)		
(106) A : The ionization (106) A : The ionization (106)	ation energy of isolated pho	sphorous is very large			
R : The ioniz	ation energy of phosphorou	s in lattice is very small			
(A)	(B)	(C)	(D)		
(107) A : Mostly transistor are used in common emitter configuration					
R: Common emitter configuration provide more current gain and small voltage gain					
(A)	(B)	(C)	(D)		
(108) A : A transistor amplifier circuit in common emitter configuration has low input impednce					
R: Base - emitter junction is forward biased					
(A)	(B)	(C)	(D)		



KEY NOTE

			-				
1	В	31	С	61	D	91	С
2	А	32	А	62	D	92	А
3	А	33	С	63	С	93	С
4	В	34	D	64	В	94	С
5	С	35	С	65	А	95	С
6	D	36	С	66	С	96	С
7	С	37	D	67	С	97	С
8	D	38	В	68	D	98	В
9	А	39	D	69	С	99	В
10	А	40	С	70	С	100	С
11	С	41	А	71	D	101	А
12	А	42	С	72	С	102	А
13	С	43	С	73	А	103	В
14	D	44	С	74	В	104	В
15	В	45	А	75	D	105	D
16	А	46	С	76	С	106	В
17	D	47	С	77	D	107	В
18	В	48	D	78	D	108	А
19	D	49	В	79	В		
20	А	50	С	80	В		
21	D	51	А	81	А		
22	С	52	А	82	D		
23	D	53	В	83	С		
24	С	54	А	84	С		
25	В	55	С	85	С		
26	С	56	D	86	С		
27	В	57	В	87	D		
28	В	58	С	88	А		
29	А	59	А	89	В		
30	D	60	D	90	С		

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Hints

(2) Out of 5 valence electrons of phosphorous, 4 are shared with Si. Fifth electron can be approximated to revolve around nucleus. Situation is like H-atom

 $En \approx -13.6/n^2 ev$

For n = 1, En = -13.6ev

E inside lattice =
$$\frac{\text{En}}{\epsilon_1^2} = \frac{-13.6}{12^2} = 0.1 \text{ ev}$$

(12)
$$\alpha = \frac{I_c}{I_e}$$
 $\therefore I_c = \alpha I_E = 9mA$

$$I_{B} = I_{E} - I_{C} = 10 - 9 = 1 \text{ mA}$$

(13)
$$\beta = \frac{\alpha}{1-\alpha}$$

- (15) Ideal diode has zero resistance in forward bias
- (22) Potential At B = Potential at D

$$(25) \quad V_{\rm rms} = \frac{V_{\rm m}}{\sqrt{2}} = \frac{V_{\rm p}}{\sqrt{2}}$$

(33) $I_c = 10 \text{mA} = 0.90 I_E$

 $\therefore I_{\rm E} \approx 11 {\rm mA}$

$$\therefore I_{B} \approx 1mA$$

- (38) Base & Emitter are forward biased & collector is reverse biased with respect to Emitter ∴ Circuit is Common emitter
- (41) $C = A + Y_1$ $Y_1 = \overline{A \cdot B}$ $\therefore C = A + \overline{A \cdot B}$
- (51) Only solar-cell generates e.m.f and it does not need bias-voltage

(54) Frequency of LC oscillator is
$$f = \frac{1}{2\pi\sqrt{LC}}$$

(55) Output voltage = voltage gain \times Input voltage. There will be a phase difference of 180° between input and output signal.

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(56)
$$\beta = \frac{\alpha}{1 - \alpha}$$
 and $A_v = \beta \frac{R_L}{r_i}$
(61) $v_d = \frac{I}{nAe}$ $\therefore v_d \alpha \frac{I}{n}$
(65) $r_i = \frac{\Delta V_{BE}}{\Delta I_B}$
(66) $\beta = \frac{\Delta I_C}{\Delta I_B}$

$$(67) \quad A_{\rm V} = \beta \frac{R_{\rm L}}{r_{\rm i}}$$

(68) Voltage gain on dB = $20 \log_{10} A_0$

(69)
$$E = \frac{v}{d} = \frac{0.6}{10^{-6}}$$
(73)
$$A_{p} = \frac{Av^{2}}{\frac{R_{L}}{r_{i}}}$$
(74)
$$\lambda = \frac{hc}{E_{g}}, f = \frac{c}{\lambda}$$

(76)
$$\alpha = \frac{I_c}{I_E} \& I_E = I_B + I_C \qquad \therefore \alpha = \frac{I_C}{I_B + I_C}$$

(78) diode
$$D_1$$
 will only conduct $\therefore I = \frac{2}{10+15}$

$$(95) \quad V_{\rm rms} = \frac{V_{\rm m}}{\sqrt{2}}$$

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